Michael Ming Kun Yang

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Skills

- Familiar with chip design flow from synthesis of RTL to netlists, physical design (place & route, timing, GDSII, library analysis), digital logic; VHDL, **Verilog**, SystemVerilog
- Knowledgeable in static timing analysis (ModelSim), chip floorplanning, clock tree synthesis, CMOS, FinFET, EM analysis, power gating
- Experienced in CAD Design tools, (**Design Compiler, IC Compiler 2, PrimeTime**), flow regression and development, revision control software (**Git,** Perforce, SVN); mastery with Vim
- Proficient with scripting in **Python**, Tcl/Tk, Bash, Csh, Perl, C, C++, Java; CUDA, OpenMP, OpenCL
- Acquainted in computer architecture in CPU, GPU, VLIW, SIMT architectures; concepts such as out-of-order execution, caching, reservation station, branch prediction, prefetching, memory coalescing
- Well versed with using and modifying simulators such as GPGPUsim, Simplescalar, InterSim
- Adept in Linux (CentOS, Redhat, Debian, Ubuntu), Unix (OS X) environment
- Accustomed to documentation of source code and new tools

Experience

06/2018 - ***Undergraduate Researcher,*** University of Toronto, Toronto, ON, Prof. Gennady Pekhimenko

- Performed microarchitectural experiments with GPGPUsim, a GPU simulator in C/C++, to model GPU performance
- Extended compatibility of simulator to support modern workloads and microbenchmarks in machine learning using frameworks such as MxNet and Tensorflow
- Thesis research in computer architecture ongoing

05/2017 - 04/2018 ***Physical Design Implementation Intern,*** Advanced Micro Devices, Sunnyvale, CA

- Enhanced hierarchical synthesis flow, improving synthesis QoR of up to 30%, to allow for modular RTL-netlist synthesis that supports SystemVerilog and Verilog
- Created Python and tcl tools to collect and characterize RTL designs and technology libraries (TSMC 7nm and GlobalFoundries 7nm) , while improving runtime of existing scripts by > 40 %
- Developed website to manage and track the performance of very large blocks of a high performance x86 microprocessor core, using Python, PHP, and JavaScript
- Developed and documented new synthesis tools and methodologies to physical designers

05/2016 - 08/2016 ***Systems Engineering Intern***, NVIDIA Corporation, Santa Clara, CA

- Executed NVIDIA Tesla P100 board level bring up, debugging, and validation
- Performed bug-tracking and failure analysis, closed all majors bugs in four month window and left with preproduction validation yield of > 90%
- Characterization of new technologies, such as wireless charging and visible light communication
- Designed schematics for NVIDIA Shield prototypes

Education

09/2014 - *06/2019* B.A.Sc., Engineering Science, **Electrical and Computer Engineering**, University of Toronto, Dean's List

Current: Computer Architecture, Introduction to Machine Learning, Foundations of Computing

Past: *Semiconductor Device Physics, Digital Electronics, Operating Systems, Algorithms and Data Structures*

Extracurriculars

09/2015 - 06/2017 ***Vision Co-lead***, Aerial Robotics, University of Toronto Aerospace Team, Toronto, ON

- Lead a team of computer vision developers
- Won 1st at the 2017 Unmanned Systems Canada — Design Phase and Judges Award for Professionalism
- Developed image progressing algorithm for polygon detection and characterization, utilizing OpenCV library, creating robot capable of autonomous image recognition